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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,122	02/05/2004	Jan-Der Guo	386998046US	3256

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EXAMINER	
SARKAR, ASOK K	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,122	GUO ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9* is/are allowed.

6)☒ Claim(s) *10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on May 3, 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 10 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo, US 6,818,531 in view of Nitta, US 5,798,537 and Erchak, US 6,831,302.

Regarding claim 10, Yoo teaches a method for forming LED, comprising the steps of:

- forming an LED epitaxial layer 25 or 125 on a provisional substrate 121;
- forming a reflecting layer 24 on said LED epitaxial layer;
- forming a metal layer 22 on said reflecting layer;
- cutting said LED epitaxial layer 25 or 125, said reflecting layer 24, and said metal layer 22 to form LED chips with reference to Figs 2 and 3(b),
- removing said provisional substrate 121 to expose surfaces of said LED chips with reference to Fig. 3(d) and;
- forming pads 139 on said surfaces of said LED chips with reference to Fig. 3(e) and associated descriptions in columns.

Yoo teaches etching the epitaxial layers by dry etching in column 1, lines 65 – 67, but fails to teach etching the epitaxial layer, the reflecting layer and the metal layer.

Nitta teaches that cutting semiconductor chips containing light emitting diodes can damage the edge portions and affect the light emission badly and therefore etching should be performed to separate them in column 6, lines 38 – 43.

Erchak also teaches that separation of LED devices should be carried out by etching instead of cutting for the benefit of reducing the potential damage to the electrical and optical properties of the patterned LEDs in column 20, lines 42 – 45.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Yoo and etch the epitaxial layer, the reflecting layer and the metal layer for the benefit of minimizing the level of stress as suggested by Yoo in column 6, lines 25 – 37 and also reduce the damaged caused to the patterned LED as suggested by Nitta in column 6, lines 38 – 43 and also by Erchak in column 20, lines 42 – 45.

Regarding claim 11, Yoo teaches the reflecting layer of combination of Ag and Au in column 5, lines 30 – 35.

Regarding claim 16, Yoo teaches the metal layer of Au, Ni, Ag and Al in column 6, lines 15 – 16.

Regarding claims 12 – 15, Yoo fails to teach the methods for depositing the metal layer.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Yoo and deposit the metal layer by various methods as described in the claims since all these methods are well known deposition methods for metallic layers.

Regarding claim 17, Yoo fails to teach the thickness of the metal layer.

However, given the substantial teaching of Yoo (see column 2, lines 25 – 32), it would have been obvious to one with ordinary skill in the art at the time of the invention

to judiciously adjust and control the thickness of the metal layer through routine experimentation and optimization to achieve optimum benefits in terms of heat dissipation (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237).

Allowable Subject Matter

6. Claims 1 – 9 are allowed.

7. The following is an examiner's statement of reasons for allowance:

Claims 1 – 9 recite, inter alia, a method of forming LED comprising the steps of etching the LED epitaxial layer formed on a provisional substrate to form the LED chips by means of photolithography, forming a reflecting layer on the LED chips, forming a metal layer on the reflecting layer, and removing the provisional substrate to expose surfaces of the LED chips. The art of record does not disclose or anticipate the above limitations of forming the metal and the reflecting layers on the etched LED chips in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Response to Arguments

8. Applicant's arguments filed May 3, 2005 have been fully considered but they are

not persuasive. The Applicant's argument in pages 11 and 12 is regarding the step of etching the epitaxial layer, the reflecting layer and the metal layer. It is alleged that Yoo teaches only cutting. It should be pointed out that cutting and etching are broadly synonymous and can be used interchangeably particularly since Yoo does not disclose the method of cutting. As mentioned earlier, Yoo also teaches etching the epitaxial layers by dry etching in column 1, lines 65 – 67 which are generally used for preparing an area for contacts. As has been described earlier in the rejection that cutting of layered chips by sawing can put lot of stress on the device and introduce defects that can damage the light emission properties of the LEDs if cutting is indeed carried out by sawing.

Conclusion

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
May 24, 2005

Primary Examiner